REMARKS

The Final Office Action mailed June 3, 2003, has been received and reviewed.

Claims 16 through 26 are currently pending in the application.

Claims 16 through 26 stand rejected.

Applicants respectfully request reconsideration of the application.

35 U.S.C. § 102(e) Rejection

Claims 16 through 26 were rejected under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Patent 6,444,921 B1).

Applicants submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Wang describes an interposer for electrically coupling two electrical components having different coefficients of thermal expansion (CTE). (Abstract). The interposer 10 electrically couples two electrical components 1 and 5 together. (FIG. 1, Col. 4, lines 6-11). Interposer 10 is composed of a first substrate 12, a second substrate 20 that is separate from first substrate 12, and a flexible circuit layer 30 spanning the two substrates. (Col. 4, lines 17-20). Flexible circuit layer 30 has a first portion which is attached to the first surface of substrate 12 and a second portion which is attached to the first surface of substrate 20. Flexible circuit layer 30 is bent such that substrates 12 and 20 face one another at their second surfaces. (Col. 4, lines 22-27). The CTEs of substrates 12 and 20 are different. (Col. 4, line 38). Interposer 10 is further comprised of a first plurality of electrical connection areas 14 over the first surface of substrate 12 and a second plurality of electrical connection areas 24 over the first surface of substrate 20. Electrical traces 35 run between areas on substrates 12 and 20 and pass through flexible circuit layer 30. (Col. 4, lines 50-56). Flexible circuit layer 30 is composed of four dielectric layers 32, 34, 36, and 38 and an inner conductive layer 33 between dielectric layers 32 and 34. A layer of traces 35 is disposed between dielectric layers 34 and 36 while an outer conductive layer 37 is disposed between

dielectric layers 36 and 38. (Col. 5, lines 12-20). Each end of each electrical trace 35 comprises a vertical via which extends from the middle conductive layer to the outer surface of flexible-circuit layer 30 and which passes through the dielectric layers 36 and 38 and outer conductive layer 37. (Col 5, lines 27-34). The vias do not extend through the substrates and no connection is made between traces 35 and substrates 12 and 20 in preferred interposer embodiments. (Col. 6, lines 8-13). One or more bypass capacitors may be formed on the first surface of substrate 12 with *connections made to it from conductive layers 33 and 37.* (Col. 6, lines 17-20, emphasis added)

By way of contrast to Wang, independent claim 16 recites elements of the invention calling for a method of packaging at least one semiconductor die in a high density arrangement comprising "providing a substrate; providing a flexible interposer including a first surface having a plurality of electrical contacts for electrically connecting at least one semiconductor die to a substrate, a second surface, and a plurality of vias extending completely through said flexible interposer from said first surface to said second surface". Wang does not describe vias extending completely through the flexible interposer.

Applicants respectfully submit that Wang fails to describe, either expressly or inherently "providing a flexible interposer including a first surface having a plurality of electrical contacts for electrically connecting at least one semiconductor die to a substrate, a second surface, and a plurality of vias extending completely through said flexible interposer from said first surface to said second surface." Wang does not describe vias that extend from "said first surface to said second surface" of the interposer. The vias in Wang extend only partially through the flexible circuit layer 30. (Col. 5, lines 27-34, 59-62). Connections to bypass capacitors formed on the first surface of substrate 12 and/or 20 from conductive layers 33 and 37 are disclosed. (Col. 6, lines 17-26). It is respectfully submitted that these connections are not vias extending completely through a flexible interposer from a first surface to a second surface. Rather, a connection from conductive layers 33 and 37 to the first surface of substrate 12 and/or 20, if made through the flexible circuit layer 30, would not comprise a via extending *completely* through the flexible circuit layer. The connection is made only to layer 37.

As Wang fails to expressly or inherently identically describe each and every element of claim 16, Applicants respectfully submit that claim 16 is not anticipated by Wang under 35 U.S.C. § 102.

Claims 17 through 22 are each allowable as depending either directly or indirectly from allowable claim 16.

Claim 21 is further allowable as Wang does not describe the element of the claimed invention calling for "said interposer folds around more than two semiconductor die in a serpentine fashion around groups including at most two semiconductor die therein." Flexible circuit layer 30 enfolds only one group of two or three CTE relieving substrates 12 and 20. Since Wang fails to describe each and every element of claim 21, Applicants respectfully submit that claim 21 is not anticipated by Wang under 35 U.S.C. § 102.

Applicant submits that independent claim 23 is allowable because Wang fails to describe, either expressly or inherently "providing an interposer including a first surface having a plurality of electrical contacts, a second surface, and a plurality of vias extending completely through said interposer from said first surface to said second surface; attaching said at least one die to said interposer to form an intermediate packaging structure" as provided in independent claim 23. As discussed above for claim 16, Wang does not provide vias that extend completely through an interposer.

Claims 24 through 26 are each allowable as depending directly from allowable claim 23.

Claim 24 is further allowable as Wang does not describe the element of the claimed invention calling for attaching *multiple semiconductor die in groups of two* semiconductor die, said semiconductor die having a back-to-back configuration, a back side of one semiconductor die substantially contacting a back side of another semiconductor die of a group. Rather, Wang describes bypass capacitors formed on the surface of a substrate used to form an interposer to electrically couple two electrical components to one another. Applicants respectfully submit that claim 24 is not anticipated by Wang under 35 U.S.C. § 102.

Applicant requests entry of this amendment for the following reasons:

The amendment is timely filed.

The amendment clearly places the application in condition for allowance.

The amendment does not require any further search or consideration.

CONCLUSION

Applicant submit that claims 16 through 26 are clearly allowable over the cited prior art for the reasons set forth herein.

Applicant requests entry of this amendment, the allowance of claims 16 through 26 ,and the case passed for issue.

Respectfully submitted,

James R. Duzan
Registration No. 28,393
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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